BENISON

JB-3

VHF FM TRANSCEIVERS

Service Manual

SPECIFICATIONS

GENERAL

. Frequency coverage	: 144.0000 ~146.0000 MHz
. Type of emission	: 8K50F3E
. Number of channels	: 100
. Power supply requirement	: 6.0 V DC (negative ground; supplied battery pack)
. Current drain (approx.)	: Transmit at 3.0 W 1.3 A
	: Receive rated audio 150 mA
	: stand-by 30 mA
. Frequency stability	: ±0.001 %
. Usable temperature range	: -10°C～+60°C
. Dimensions (projections not included)	: 58(W)×100(H)×32(D) mm
. Weight (with ant., BP-318)	: 220 g

TRANSMITTER

. RF output power (at 6.0 V DC)	: 3 W
. Modulation system	: Variable reactance frequency modulation
. Maximum frequency deviation	: ±2.5 kHz
. Spurious emissions	: 70 dB typical
. Adjacent channel power	: 60 dB typical
. Transmitter audio distortion	: Less than 3% at 1 kHz, 40% deviation

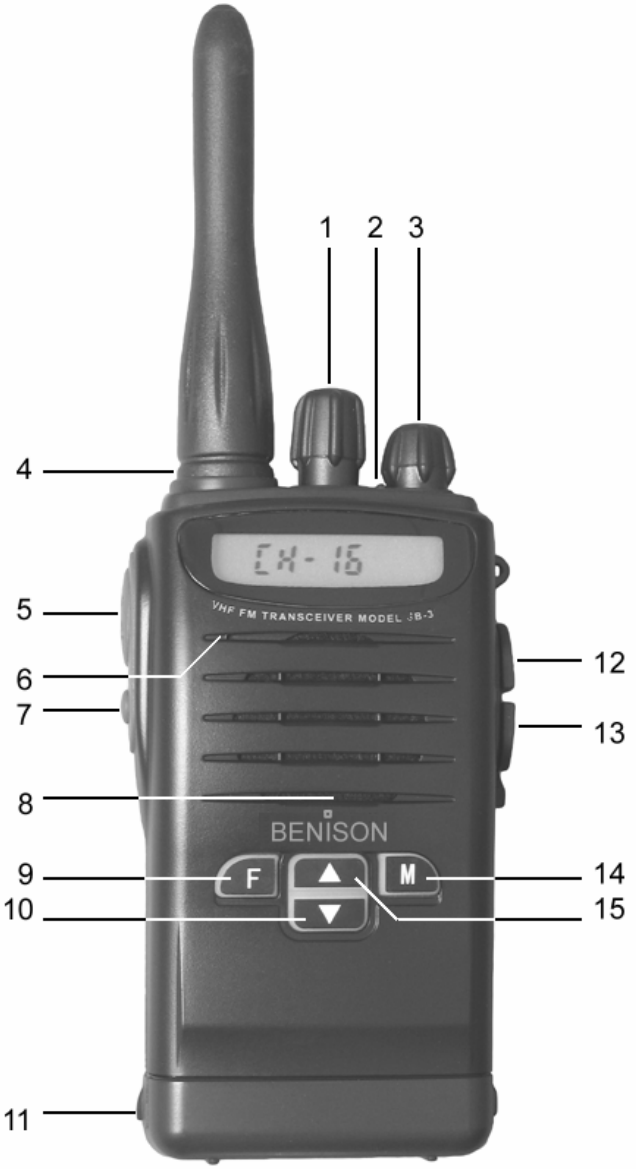
RECEIVER

. Receive system	: Double conversion superheterodyne system
. Intermediate frequencies	: 1st 21.400 MHz / 2nd 455 kHz
. Sensitivity	: 0.18 μV at 12 dB SINAD (typical)
. Squelch sensitivity	: 0.25 μV at threshold (typical)
. Adjacent channel selectivity	: 65 dB (typical)
. Spurious response rejection	: 70 dB (typical)
. Intermodulation rejection ratio	: 70 dB (typical)
. Hum and noise	: 40 dB (typical)
. Audio output power (at 6.0 V DC)	: 300 mW typical at 5% distortion with an 8 ohm load

All stated specifications are subject to change without notice or obligation.

50 CTCSS TONES SQ. (Hz)									
NO.	TONE	NO.	TONE	NO.	TONE	NO.	TONE	NO.	TONE
1	67.0	11	94.8	21	131.8	31	171.3	41	203.5
2	69.3	12	97.4	22	136.5	32	173.8	42	206.5
3	71.9	13	100.0	23	141.3	33	177.3	43	210.7
4	74.4	14	103.5	24	146.2	34	179.9	44	218.1
5	77.0	15	107.2	25	151.4	35	183.5	45	225.7
6	79.7	16	110.9	26	156.7	36	186.2	46	229.1
7	82.5	17	114.8	27	159.8	37	189.9	47	233.6
8	85.4	18	118.8	28	162.2	38	192.8	48	241.8
9	88.5	19	123.0	29	165.5	39	196.6	49	250.3

CONTROL AND CONNECTIONS



1. **VOLUME CONTROL /POWER SWITCH**
2. **TX INDICATOR**
3. **SQUELCH CONTROL**
4. **ANTENNA JACK**
5. **PTT BUTTON**
6. **INTERNAL MICROPHONE**
7. **MONI/FUNCTION BUTTON**
8. **INTERNAL SPEAKER**
9. **F BUTTON**
10. **DOWN BUTTON**
11. **BATTERY PACK**
12. **SPEAKER JACK**
13. **MICROPHONE JACK**
14. **M BUTTON**
15. **UP BUTTON**

CIRCUIT DESCRIPTION

1) Receiver System

The receiver system is a double superheterodyne system with a 21.4MHz first IF and a 455kHz second IF.

1. Front End

The received signal at any frequency in the 144.0000 to 146.0000-MHz range is passed through the low-pass filter (L29, L28, L14, C169, C166, C175 and C127) and tuning circuit (L12 and C162), and amplified by the RF amplifier (Q29). The signal from Q29 is then passed through the tuning circuit (L9 and L11 varicaps C163 and C161) and converted into 21.4MHz by the mixer (Q28).The tuning circuit, which consists of L13.

2. IF Circuit

The mixer mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (FL3, FL2) selects 21.4MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q17) then amplifies the signal of the selected frequency.

3. Demodulator Circuit

After the signal is amplified by the first IF amplifier (Q17), it is input to pin 16 of the demodulator IC (IC10). The second local signal of 20.945MHz, which is oscillated by the internal oscillation circuit in IC10 and crystal (X3). Then, these two signals are mixed by the internal mixer in IC10and the result is converted into the second IF signal with a frequency of 455kHz. The second IF signal is output from pin 3 of IC14 to the ceramic filter (FL1), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC10 through pins 5.The second IF signal input via pin 5 is demodulated by the internal limiter amplifier and quadrature detection circuit in IC10, and output as an audio signal through pin 9.

4. Audio Circuit

AF signals from the FM IF IC (IC10, pin 9) are applied to the AF amplified (IC9, pin 6) via the AF filter circuit (Q30,Q31). The output signals from Q31 are applied to the AF power amplifier (IC1, pin 4) after being passed through the [VOL] control (W1).The applied AF signals are amplified at the AF power amplifier circuit (IC1, pin 4) to obtain the specified audio level. The amplified AF signals, output from pin 10, are applied to the internal speaker (SP1) as the “SP” signal via the [SP] jack when no plug is connected to the jack.

5. Squelch Circuit

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch switches the AF mute switch. A portion of the AF signals from the FM IF IC (IC10, pin 9) are applied to the active filter section (IC10, pin 8) where noise components are amplified and detected with an internal noise detector. The active filter section amplifies noise components. The filtered signals are rectified at the noise detector section and converted into “NOIS” (pulse type) signals at the noise comparator section. The “NOIS” signal is applied to the CPU(IC3, pin 11). The CPU detects the receiving signal strength from the number of the pulses, and outputs an “AFB” signal from pin 9. This signal controls the mute switch (Q1,Q3) to cut the AF signal line.

2) Transmitter System

1. MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit. The AF signals from the microphone are applied to the microphone amplifier circuit (IC2, pin 3). The amplified AF signals are passed through the low-pass filter circuit (pins 5, 6). The filtered AF signals are applied to the modulator circuit after being passed through the W3.

2. MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signal.

The audio signals change the reactance of a diode (D19) to modulate an oscillated signal at the VCO circuit (Q27).The oscillated signal is amplified at the buffer-amplifiers (Q21,Q24), then applied to the T/R switching circuit (D9, D10).

3. DRIVE/POWER AMPLIFIER CIRCUITS

The signal from the VCO circuit passes through the T/R switching circuit (D9) and is amplified at the buffer (Q19),drive (Q32) and power amplifier (Q26) to obtain 3W of RF power (at 6.0 V DC). The amplified signal passes through the antenna switching circuit (D11), and low-pass filter and is then applied to the antenna connector.

3) PLL Synthesizer Circuit

1. PLL

The dividing ratio is obtained by sending data from the CPU (IC3) to pin 15 and sending clock pulses to pin 16 of the PLL IC (IC7). The oscillated signal from the VCO is amplified by the buffer (Q22) and input to pin 12 of IC7. Each programmable divider in IC7 divides the frequency of the input signal by N according to the frequency data, to generate a comparison frequency of 12.5kHz.

2. PLL Loop Filter Circuit

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 10) of IC7 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the varicap of the VCO unit for oscillation frequency control.

3. VCO Circuit

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.The PLL circuit contains the VCO circuit (Q25, Q27). The oscillated signal is amplified at the buffer-amplifiers (Q21, Q22) and then applied to the PLL IC (IC7). The PLL IC contains a prescaler, programmable counter, programmable divider and phase detector, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency. If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency. A portion of the VCO signal is amplified at the buffer-amplifier (Q24) and is then applied to the receive 1st mixer (Q28) or transmit buffer-amplifier circuit (Q19) via the T/R switching diode (D9, D10).

4) CPU and Peripheral Circuits

1. LCD Display Circuit

The IC5 turns ON the LCD via segment and common terminals with 1/4 the duty and 1/3 the bias, at the frame frequency is 100Hz.

2. Display Lamp Circuit

When the key is pressed, “H” is output form pin 10 of CPU (IC3) to the bases of Q4 and Q14. Q15 then turn ON and the LED (D1,D2,D12,D14) light.

3. CTCSS Encoder

The IC6 is equipped with an internal tone encoder, The tone signal (67.0 to 254.3Hz) is output from pin 18 of the IC6 to the varicap (D19) of the VCO for modulation.

4. CTCSS Decoder

The voice band of the AF output signal from pin 9 of IC10 is cut by sharp active filter IC6 and amplified, then led to pin 4 of CPU. The input signal is compared with the programmed tone frequency code in the CPU. The squelch will open when they match.

ADJUSTMENT PROCEDURES

Note:

It is assumed that the unit is supplied with a regulated 8.4 volts during the adjustment procedure. Do not use a metal screw driver to adjust the ferrite cores as it causes variations in the inductance whilst adjustments are being performed. Use of the wrong size trimming tools can cause damage to the cores. A plastic or ceramic trimming tool is recommended.

ADJUSTMENT

1) Required Test Equipment

The following items are required to adjust radio parameters:

1. Regulated power supply
Supply voltage: 5~14V DC
Current: 3A or more

2. Digital multimeter
Voltage range: FS = Approx. 20V
Current: 10A or more
Input resistance: High impedance

3. Oscilloscope
Measurable frequency: Audio frequency

4. Audio dummy load
Impedance: 8 ohm
Dissipation: 1W or more
Jack: 3.5mm

5. SSG
Output frequency: 300MHz or more
Output level: -20dBu/0.1uV ~120dBu/1V
Modulation: FM

6. Spectrum Analyzer
Measuring range: Up to 2GHz or more

7. Power meter
Measurable frequency: Up to 300MHz
Impedance: 50, unbalanced
Measuring range: 0.1W ~10W

8. Audio volmeter
Measurable frequency: Up to 100kHz
Sensitivity: 1mV to 10V

9. Audio generator
Output frequency: 67Hz to 10kHz
Output impedance: 600, unbalanced

10.Distortion meter/SINAD meter
Measurable frequency: 1kHz
Input level: Up to 40dB
Distortion: 1% ~100%

11.Frequency counter

Measurable frequency: Up to 300MHz

Measurable stability: Approx. ±0.1ppm

12.Linear detector

Measurable frequency: Up to 300MHz

Characteristics: Flat

CN: 60dB or more

Note

Standard modulation: 1kHz ±2.5kHz/DEV

Reference sensitivity: 12dB SINAD

Specified audio output level: 300mW at 8

Adjustment Mode

TX OUTPUT POWER ADJUSTMENT

STEP	CONDITIONS	ADJUST	READINGS
1	Set the power supply voltage to 6.0V	—	—
2	Connect antenna output to a RF power meter	—	—
3	Press the PTT switch	L25,L20,L14	Set RF output between 3W Supply current to be less than 1300mA

MODULATION ADJUSTMENT

STEP	CONDITIONS	ADJUST	READINGS
1	Connect the antenna output via a suitable RF attenuator to a modulation analyzer	—	—
2	Apply 1000Hz at a level of 5.0mV to the microphone jack	—	—
3	Press the PTT switch	W3	Modulation analyzer reading 1.5kHz (+/-0.2KHz)
4	Increase the modulation signal level to 50mV	W3	Modulation analyzer reading 2.5kHz (+/-0.1KHz)

SERVICING AND REPAIR

RF RECEIVE CIRCUITS

1. Ensure that the transceiver has not been switched to the battery saving mode.
2. Carefully check that all connectors are in a good condition. Check that the power supply voltage(IC8) of the receiver circuit is approximately 4.5V.
3. If the correct gain is measured then check that the bias of Q29 is Vs=2V and Vd=4.2V. Remove the RF shield on the VCO circuit and check the signal level at the collector of Q21, the local oscillator output, the signal level should be around -10dBm and the spectrum purity should be good.
4. Check that the bias voltages of the IF amplifier, Q17, are typically Vb=0.68V and Vc=3.0V.

LOCAL OSCILLATOR

If the output level of Q25 the local oscillator output, is incorrect or the spectrum purity is poor. Then the PLL circuit may not be fully locked.

1. Check that the bias voltages Q25 are typically Vb=2V, Ve=1.0V.
2. Switch the transceiver to the operating channel required. Use the frequency counter to measure that the collector output of Q21 is the required frequency minus 21.4MHz (+/-100Hz).
3. Switch the transceiver to the required operating frequency. Remove the screen and using a RF probe connect a spectrum analyzer to the collector of Q24(C). Press the PTT. The output should be at the required frequency +/-100Hz and at a level of approximately +10dBm.

TRANSMIT CIRCUIT

1. Carefully check that all connectors are in good condition and check that the power supply voltage is correct.
2. Using the frequency counter to check that the operating frequency is correct. If not, check whether the PLL is locked. If the PLL is unlocked, check the local oscillator circuit. If the PLL is locked, check that the RF output is correct. If not, check from Q21 Q24 Q19 Q32 Q26 stage by stage to assure that the signal levels are correct. First check the bias voltage of each stage and then try to find any voltages which are out of tolerance.

VOLTAGE REGULATION CIRCUIT

Apply 6.0 volts to the power input jack, Measure the collector voltage of IC8. The normal value should be approximately 5.0 volts. The voltage at the collector of IC8 should hold are approximately 5.0 volts.

AUDIO OUTPUT

1. Connect a signal generator set to the required frequency at an output level of 1mV, deviated with a 1kHz tone and 1.5kHz deviation to the antenna socket. Connect a probe to pin 10 (the output pin) of

IC1. If the transceiver is operating correctly a 1kHz sine wave should be present.

2. If not, then use the oscilloscope to check the second local oscillator to assure that it is operating correctly. A probe connected to the case of X3 or pin 1 of IC10 should detect the presence of a 20.945MHz sine wave. If not, then X3 may have failed.
3. If a 1kHz signal is measured at pin 9 of IC10 then decrease the output level of the signal generator to 0.35uV. If the 1kHz audio signal disappears when the RF level is decreased to this level, then IC10 may be faulty.
4. If IC10 appears okay, then check IC1 are correct. Check for the presence of a 1kHz audio signal at the collector of the pin10.
5. Check pin 4 of IC1 to see if there is a 1kHz audio signal present. Check pin 10 of IC1 for a presence of a large 1kHz audio signal. If the audio output signal is too small or not present then IC1 may be faulty.

CONTROL PROBLEM

If the LCD display becomes faulty then check the drive IC5.

MEMO